

# PATENT ABSTRACTS OF JAPAN

(11) Publication number : 10-322185

(43) Date of publication of application : 04.12.1998

(51)Int.Cl. H03K 17/08

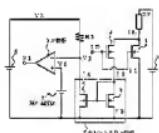
H02H 3/087

H03K 17/12

(21)Application number : 09-126948 (71)Applicant : NEC CORP

(22) Date of filing : 16.05.1997 (72) Inventor : IYODA MORITAKA

(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE



(57) Abstract:

PROBLEM TO BE SOLVED: To improve the detection accuracy of abnormality, such as the overload, etc., and also to improve the resistance to the noise interference by converting the change of an extracted load current into a current change voltage signal and comparing this voltage signal with a prescribed reference voltage to output a comparison signal.

SOLUTION: A comparator 7 compares the detection voltage V1 with the reference voltage V0 and outputs a comparison signal S1, in response to the difference between the V1 and V0. The shape of each element and a circuit constant are set, so that the V1 is equal to the V0, when the load current IL of its upper limit value flows into the load Z2. Thus, the relation of values between the V1 and V0 is inverted between a normal state in which the current IL is smaller than its set upper limit value and an overload state where the current IL exceeds its set upper limit value. As a result, the output level of the signal S1 has a large change, and the state of an FET 1 is detected. Furthermore, the influence of the current error caused at a current mirror circuit can be reduced, since this circuit has a single stage.

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#### LEGAL STATUS

[Date of request for examination] 16.05.1997

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 3225887

[Date of registration] 31.08.2001

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right] 31.08.2005

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CLAIMS

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[Claim(s)]

[Claim 1] The semiconductor integrated circuit equipment which carries out [ having an electrical-potential-difference comparison means compares the semiconductor device for an output which is connected to a load and controls the load current of this load, a load current change extract means extract a changed part of said load current, and a current-potential conversion means change a changed part of said extracted load current into a current change voltage signal with the reference voltage which determined as said current change voltage signal beforehand, and output a comparison signal, and ] as the description.

[Claim 2] The 2nd FET by the ratio as which parallel connection of each of a drain and the gate was carried out to the drain of the 1st FET and each of the gate which are said semiconductor device, and gate area determined it beforehand with said load current change extract means smaller than said 1st FET, Semiconductor integrated circuit equipment according to claim 1 characterized by having the current Miller circuit which the input edge connected to the source of said 2nd FET, and equipping said current potential conversion means with the resistance which the end connected to the outgoing end of said current Miller circuit, and the other end connected to the power source.

[Claim 3] Semiconductor integrated circuit equipment according to claim 1 characterized by having further a driving signal cutoff means to answer supply of

said comparison signal and to intercept the driving signal of said semiconductor device.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention relates to the semiconductor integrated circuit equipment for Power IC which integrated the control system and the output stage component of a high current about semiconductor integrated circuit equipment.

[0002]

[Description of the Prior Art] It has the protection feature for preventing conventionally that a power semi-conductor breaks by the overcurrent, a short circuit, etc. in the semiconductor integrated circuit using this kind of power semi-conductor.

[0003] If drawing 3 which shows the 1st conventional semiconductor integrated circuit equipment given [ including the monitor signal generation circuit for this kind of protection features ] in JP,1-193909,A with a circuit diagram is referred to

FET1 which is the voltage-controlled power semiconductor device by which the drain connected this 1st conventional semiconductor integrated circuit equipment to the load Z2, FET2 which is a semiconductor device with the small current capacity in which a drain and the gate carried out parallel connection to the source and the gate of FET1, respectively, Current Miller circuit 101 which consists of the transistors 33 and 34 of an NPN form, It has current Miller circuit 102 which consists of the transistors 35 and 36 of an PNP form, the current source 37 which supplies reference current  $I_0$  to a transistor 36, the power source 8 which supplies a power source to current Miller circuit 102, and the power source 9 of FET 1 and 2.

[0004] Next, if actuation of the 1st conventional semiconductor integrated circuit equipment is explained with reference to drawing 3 , the drain current of FET2 will be received in current Miller circuit 101, and the voltage signal  $S_1$  corresponding to differential current will be outputted to an output terminal TO as compared with the output of current Miller circuit 102 of reference current  $I_0$  response.

[0005] Since this circuit is connected so that power FET 1 and FET2 with small current capacity may be arranged in parallel, the current  $I_L$  which flows for a load Z2 is divided into the currents  $I_1$  and  $I_2$  which serve as a rate of surface ratio of FET1 and FET2, and each of these currents  $I_1$  and  $I_2$  will be divided into FET1 and FET2, respectively, and will flow. If a current  $I_2$  flows to FET2, when this current  $I_2$  flows into the transistor 33 of current Miller circuit 101, to a transistor 34, the current  $I_3$  decided by the rate of surface ratio of transistors 33 and 34 will flow. Moreover, the current which flows to the transistor 36 of current Miller circuit 102 serves as a fixed value according to the constant current source 37, and the current  $I_4$  decided by the rate of surface ratio of transistors 35 and 36 flows to a transistor 35. Therefore, there is no capacity to pass only the current  $I_4$  of a certain constant value in a transistor 35 to the current  $I_3$  which changes to a transistor 34 in proportion to the condition of a current  $I_1$  of flowing for a load R2 flowing. Therefore, in order for the surplus of a current to occur since it becomes

impossible for a transistor 34 to be able to continue passing the programmed current  $I_4$  of a transistor 35 when a current  $I_3$  is small, and to abolish this surplus current, in order that the operating point may move from a transistor 35 to a saturation region from a non-saturation region compared with a current  $I_4$ , the voltage level  $S_1$  of an output terminal  $TO$  rises. Conversely, in order that the operating point may move from a transistor 34 to a saturation region from a non-saturation region compared with a current  $I_4$  so that lack of a current may occur since a transistor 34 cannot be passed more than programmed-current  $I_4$  and this insufficiency may be lost, when a current  $I_3$  is large, the voltage level  $S_1$  of an output terminal  $TO$  descends.

[0006] As explained above, the voltage level  $S_1$  of an output terminal  $TO$  changes with the size relation of the current values  $I_3$  and  $I_4$  which flow to transistors 34 and 35. thereby -- the reference current value  $I_0$  and current Miller circuit 101,102 -- overload condition detection of FET1 is realized using change of the voltage level  $S_1$  of the output terminal  $TO$  when the current  $I_1$  which flows to FET1 becomes beyond a programmed-current value by setting up each transistors 33 and 34 of each and the rate of surface ratio of 34 and 36.

[0007] Next, if drawing 4 which shows the 2nd conventional semiconductor integrated circuit equipment given in JP,6-244693,A similarly to drawing 3 and a common component with a circuit diagram using common alphabetic character/figure is referred to FET 1 and 2 with this 2nd conventional as common semiconductor integrated circuit equipment which corrected and carried out parallel connection of the source and the gate comrade as the 1st conventional technique, To the load  $Z_2$  between the drain of FET1, and a power source 9, and a power source 9, in addition, the resistance  $R201$  for criteria which connects between the drain of FET2, and a power source 9, and generates the reference voltage  $V_0$  corresponding to a drain current of FET2, It has the comparator 201 which compares the load electrical potential difference  $V_1$  and reference voltage  $V_2$  which were produced for the load  $Z_2$ , and outputs the comparison signal  $VS$ , and the bias control circuit 202 which controls the bias voltage of the gate of FET

1 and 2.

[0008] Next, if actuation of the 2nd conventional semiconductor integrated circuit equipment is explained with reference to drawing 4 , FET1 and FET2 are the on resistance corresponding to the inverse numbers K1 and K2 ( $K1 < K2$ ) of each rate of surface ratio, respectively. Moreover, it will usually always be in a condition with the higher, the electrical potential difference  $V1$  between source drains, i.e., the load electrical potential difference, of FET1, electrical potential difference  $V0$  between source drains of FET2, i.e., reference voltage, to the resistance  $r2$  of the load  $Z2$  of FET1 at the time of a load by setting up the resistance  $r1$  of the load resistance  $R201$  of FET2 with  $\{(K2-1) \times R2\}$ . These electrical potential differences  $V1$  and  $V0$  are supplied to forward [ of a comparator 201 ], and a reversal input, and the comparison signal  $S1$  outputs  $L$  level. The bias control circuit 202 answers  $L$  level of the comparison signal  $S1$ , and a transistor 21 intercepts it, and it usually holds bias voltage  $B$  of FET 1 and 2 on level. When [ this ] the resistance of a load  $Z2$  usually falls by a certain cause to loaded condition, the direction of the load electrical potential difference  $V1$  will be in a high condition from reference voltage  $V0$ . A comparator 201 answers lifting of the load electrical potential difference  $V1$ , reverses the comparison signal  $S1$ , and is taken as  $H$  level.  $H$  level of this comparison signal  $S1$  is answered, the transistor 22 of the bias control circuit 202 flows, and bias voltage  $B$  is dropped. Thus, detection of loaded condition and abnormality loaded condition is usually realized by comparing electrical potential differences  $V1$  and  $V0$  by the comparator 201.

[0009] Next, if drawing 5 which shows the 3rd conventional semiconductor integrated circuit equipment given in JP,3-195212,A with a block to drawing 3 and a common component using common alphabetic character/figure is referred to FET1 with this 3rd conventional as common semiconductor integrated circuit equipment as the 1st conventional technique, The electrical-potential-difference detector 301 which connects between the gate sources of FET1 and outputs the detection electrical potential difference  $VG$  corresponding to the electrical

potential difference between the gate sources, It has the gate drive circuit 302 which amplifies an input signal D by control of the comparison signal S2, and supplies the drive signal G of the gate of FET1, the comparator 303 which compares reference voltage V0 with an electrical potential difference VG, and outputs the comparison signal S2, and the reference voltage generator 304 which generates reference voltage V0.

[0010] Next, if actuation of the 3rd conventional semiconductor integrated circuit equipment is explained with reference to drawing 5 , this circuit will perform desired current limiting by using the saturation area property of the electrical potential difference between the gate sources, and a drain current by carrying out adjustable [ of the level of the output G of a gate drive circuit 302 ]. First, a comparator 303 compares the gate detection electrical potential difference VG with reference voltage V0, and it controls the drive signal G so that the electrical potential difference between the gate sources does not become larger than reference voltage V0. Thus, by setting up the electrical potential difference between gate drains, it becomes impossible for the drain current of FET1 to pass beyond the current value decided by the static characteristic, and it enables a limit of the drain current of FET1.

[0011]

[Problem(s) to be Solved by the Invention] The current error produced in each of two steps of current Miller circuits affected the current value which flows to the semiconductor device of a reference current value and the small current capacity for overcurrent detection, respectively, and the 1st conventional semiconductor integrated circuit equipment mentioned above had the fault of becoming a cause with error.

[0012] Moreover, in the usual bipolar transistor which constitutes the above-mentioned current Miller circuit, it is several Mohm order, therefore the impedance in an output terminal was set to several M omega, and the impedance between the emitter collectors in an active region had the fault of the switching noise generated at the time of switching having affected an output

signal line by capacity coupling, and generating malfunction.

[0013] Moreover, the 2nd conventional semiconductor integrated circuit equipment had the fault of a latch rise etc. having occurred and resulting in component destruction, in order for the electrical potential difference more than supply voltage to join the input terminal of a comparator according to back EMF generated at the time of a turn-off, when a load contains an inductance component.

[0014] Furthermore, even if the power consumption in a power semi-conductor increased remarkably and the 3rd conventional semiconductor integrated circuit equipment has prevented destruction by the overcurrent in order to make it operate in a saturation region although it used the saturation characteristics of an electrical-potential-difference actuation mold semiconductor device, there was a fault of resulting in a thermal runaway.

[0015] Even if the object of this invention is a load which the trouble which the above-mentioned conventional technique has is solved, and malfunction detection precision, such as an overload, removes a thermal runaway factor to noise interference strongly [ it is high and ], and contains an inductance component, it is to offer the semi-conductor circuit apparatus which enables condition detection of a power semiconductor device.

[0016]

[Means for Solving the Problem] It has an electrical-potential-difference comparison means compares the semiconductor device for an output which is connected to a load and controls the load current of this load, a load current change extract means extract a changed part of said load current, and a current-potential conversion means change a changed part of said extracted load current into a current change voltage signal with the reference voltage beforehand determined as said current change voltage signal, and output a comparison signal, and the semiconductor integrated circuit equipment of this invention is constituted.

[0017]

[Embodiment of the Invention] If drawing 1 which shows the gestalt of operation of the 1st of this invention to drawing 9 and a common component with a circuit diagram using common alphabetic character/figure is referred to, next, the semiconductor integrated circuit equipment of the gestalt of this operation shown in this drawing FET1 which is the 1st conventional technique which carried out parallel connection of a drain comrade and the gate comrade, and a common component for power, and FET2 which is a small current component for detection, To the power source 8 which supplies an electrical potential difference V3, the power source 9 which supplies the load current IL, and the resistance R2 for loads, in addition, current Miller circuit 5 which consists of FET 3 and 4 which is an N-channel metal oxide semiconductor form transistor, The resistance R1 which connects between a power source 8 and the drain of FET4, and generates the detection electrical potential difference V1, It has the source 6 of reference voltage which supplies reference voltage V0, and the comparator 7 which inputs reference voltage V0 into a plus input, inputs the detection electrical potential difference V1 into a reversal input, respectively, compares these electrical potential differences V0 and V1, and outputs the comparison signal S1.

[0018] Next, when actuation of the gestalt of this operation is explained with reference to drawing 1 , as mentioned above with the 1st conventional technique, first, the currents I1 and I2 of FET1 and FET2 are distributed so that the load current IL which flows a load Z2 may be changed with the ratio of the components area A1 and A2 of FET1 and FET2, and are expressed with a degree type, respectively.

[0019]

$$I1=ILxA1/(A1+A2) \dots \dots \dots (1)$$

$$I2=ILxA2/(A1+A2) \dots \dots \dots (2)$$

A current I2 flows to FET3 of current Miller circuit 5, and the current I4 of each component area A3 of FET 3 and 4 and the degree type determined by the ratio of A4 flows to FET4.

[0020]

$$I_4 = I_2 \times A_4 / (A_3 + A_4) \dots (3)$$

If this current  $I_4$  flows to the resistance  $R_1$  between FET4 and a power source 8 and the resistance of this resistance is set to  $R_1$ , the detection electrical potential difference  $V_1$  expressed with a degree type at the joint  $N_1$  which are resistance  $R_1$  and FET4 and a node will generate it.

[0021]

$$V_1 = V_3 - R_1 \times I_4 \dots (4)$$

$$= V_3 - [R_1 L_x A_2 \times A_4 / ((A_1 + A_2) \times A_3)] \dots (5)$$

That is, the detection electrical potential difference  $V_1$  changes according to the condition of the load current  $I_L$ .

[0022] A comparator 7 compares the detection electrical potential difference  $V_1$  with reference voltage  $V_0$ , and outputs the comparison signal  $S_1$  corresponding to the size relation of these electrical potential differences  $V_0$  and  $V_1$  to an output terminal  $T_0$ .

[0023] Here, when the upper limit of the load current  $I_L$  flows for a load  $Z_2$ , the configuration and circuit constant of each component are set up so that the detection electrical potential difference  $V_1$  and reference voltage  $V_0$  may become equal. When the load current  $I_L$  is smaller than a setting-out upper limit, i.e., the load current  $I_L$  flows with a normal state by this exceeding a setting-out upper limit, and the size relation between the detection electrical potential difference  $V_1$  and reference voltage  $V_2$  is reversed in the state of an overload, and the output level of the comparison signal  $S_1$  changes a lot, condition detection of FET1 is performed.

[0024] That is, in a normal state, since the detection electrical potential difference  $V_1$  is smaller than reference voltage  $V_0$ , the comparison signal  $S_1$  serves as L level. In the state of an overload, since the detection electrical potential difference  $V_1$  becomes larger than reference voltage  $V_0$  at reverse, the comparison signal  $S_1$  is reversed on H level.

[0025] It considers as a concrete numerical example, and the resistance of 10:1 and resistance  $R_1$  is set to 2.5kohm, and the electrical potential difference  $V_3$  of

2.5V and a power source 8 is set [ surface ratio A1:A2 of FET 1 and 2 / surface ratio A3:A4 of FET 3 and 4 of 999:1 current Miller circuit 5 ] to 5V for reference voltage V0. Moreover, as a load Z2, the inductance of direct-current equivalent resistance low enough shall be connected.

[0026] A driving signal ID is supplied to FET 1 and 2 in this condition, from a load Z2, the load current IL which increases with time amount progress begins to flow, and FET 1 and 2 assumes the condition that the load current IL reached to 9A, when it will be from a cut off state in switch-on. At this time, to FET 1 and 2, the currents I1 and I2 according to the rate of surface ratio flow, a current I1 is set to 8991mA, and a current I2 is set to 9mA from (1) and (2) types. Since a current I2 flows to current Miller circuit 5 as it is, the current I4 of 9mA and FET4 is set to 0.9mA from (3) and (4) types by the current I3 of FET3. This current I4 is transformed into the detection electrical potential difference V1 by resistance R1, and this electrical potential difference V1 is set to 2.75V from (4) types, and is supplied to the reversal input of a comparator 7. On the other hand, since the plus input electrical potential difference of a comparator 7 is 2.5V of reference voltage V0, a comparator outputs L level.

[0027] Next, it passes in time than the above-mentioned circuit condition, and the condition of current 10 A+alpha that the load current IL exceeds 10A slightly is assumed. At this time, in 9990 mA+alpha 1 and a current I2, 10 mA+alpha 2 and a current I3 serve as 10 mA+alpha 2, and a current I4 serves as [ a current I1 ] 1 mA+alpha 3. This current I4 is transformed into the detection electrical potential difference V1 by resistance R1, and this electrical potential difference V1, i.e., the reversal input voltage of a comparator 7, becomes 2.5 V-alpha 4. On the other hand, the plus input electrical potential difference of a comparator 7 is still reference voltage 2.5V, since the electrical potential difference of a plus input becomes high slightly rather than the electrical potential difference of a reversal input, it is reversed and the comparison signal S1 serves as H level. By supervising the level of this comparison signal S1, whether FET's1 being in the overcurrent condition and a condition are detectable.

[0028] Moreover, to constituting from the 1st conventional technique in two steps of current Miller circuits, with the gestalt of this operation, since the number of current Miller circuits is one, the effect of the current error produced in current Miller circuit can be reduced. Moreover, there is no location which serves as a high impedance called several Mohm order all over the circuit of the gestalt of this operation, and the margin to malfunction by a switching noise etc. can be expanded.

[0029] Furthermore, it is possible for a load not to be limited to resistance like the 2nd conventional technique, and to also treat an inductance load.

[0030] Moreover, in the gestalt of this operation, an NPN bipolar form transistor may be used instead of using FET of an N-channel metal oxide semiconductor form as a transistor which constitutes current Miller circuit.

[0031] Next, when drawing 2 which shows the gestalt of operation of the 2nd of this invention similarly to drawing 1 and a common component with a circuit diagram using common alphabetic character/figure is referred to, the point of difference with the gestalt of operation of the 1st of the gestalt of this operation shown in this drawing is having added further the cutoff circuit 10 which answers the reversal to H level of the comparison signal S1, and intercepts the driving signal ID of FET 1 and 2.

[0032] The cutoff circuit 10 is equipped with AND circuit A1 of 2 inputs which take the AND of the drive signal D and the latch signal L which are supplied from a latch circuit F1 and the actuation circuits 11, such as an RS flip flop which latches the comparison signal S1 and outputs the latch signal L, and generate a driving signal ID.

[0033] If actuation is explained, a latch circuit F1 will set an initial-state, i.e., signal, Q bar to H level by reset-signal R at the time of starting. A latch circuit F1 answers the carrier beam comparison signal S1 in supply, latches this signal S1 to Input S, and supplies a reversal output-signal Q bar to one input of AND circuit A1. AND circuit A1 takes an AND with the carrier beam drive signal D for supply to the input of this signal Q bar and another side, and outputs a driving signal ID

to it. In the state of normal operation, as mentioned above, since it is L level, a signal Q bar serves as H level, and the comparison signal S1 passes the drive signal D, and outputs AND circuit A1 as a driving signal ID. Therefore, FET 1 and 2 operates according to the level of the drive signal ID.

[0034] Next, in the state of an overload, since the comparison signal S1 serves as H level and a signal Q bar serves as L level, AND circuit A1 intercepts the drive signal D, therefore a driving signal ID. Consequently, FET 1 and 2 will be in a cut off state, and protected operation is realized.

[0035] When FET 1 and 2 intercepted, it becomes impossible to supply a current to loads 3 and FET [ Z2 and ] 4. However, when the comparison signal S1 changes from H level to L level again, almost simultaneously with cutoff of these FET 1 and 2, the input S of a latch circuit F1 changes from H level to L level. However, a signal Q bar will continue holding L level until reset-signal R is inputted, and regardless of the drive signal D, FET 1 and 2 continues holding a cut off state, and protects FET 1 and 2.

[0036] Like the 3rd conventional technique, the circuit of the gestalt of this operation does not use the saturation characteristics of Power FET, and a component does not necessarily destroy it by generation of heat by the rapid increment in power consumption for actuation of making power FET itself intercept.

[0037]

[Effect of the Invention] As explained above, since the semiconductor integrated circuit equipment of this invention is equipped with the load current change extract means, the current potential conversion means, and the electrical-potential-difference comparison means, and it reduced current Miller circuits to one step, it has the effectiveness of it being said that condition detection of a semiconductor device is possible with high degree of accuracy.

[0038] Moreover, since there is no part used as a high impedance all over a circuit, it is effective in the malfunction margin by disturbance noises, such as a switching noise, being made greatly.

[0039] Moreover, since it changes and detects on an electrical potential difference after not carrying out direct detection of the potential change of a load but extracting as current change and the effect of a load impedance condition is avoidable, it is effective in not only resistance but an inductance being connectable as a load.

[0040] Furthermore, a voltage-controlled semiconductor device is not controlled by the saturation region, but it is effective in the ability to prevent the thermal runaway by the increment in loss within a semiconductor device by intercepting thoroughly.

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DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1] It is the circuit diagram showing the gestalt of operation of the 1st of the semiconductor integrated circuit equipment of this invention.

[Drawing 2] It is the circuit diagram showing the gestalt of operation of the 2nd of the semiconductor integrated circuit equipment of this invention.

[Drawing 3] It is the circuit diagram showing an example of the 1st conventional semiconductor integrated circuit equipment.

[Drawing 4] It is the circuit diagram showing an example of the 2nd conventional semiconductor integrated circuit equipment.

[Drawing 5] It is the block diagram showing an example of the 3rd conventional semiconductor integrated circuit equipment.

[Description of Notations]

1-4 FET

21, 33-36 Transistor

5,101,102 Current Miller circuit

6 Source of Reference Voltage

7,201,303 Comparator

8 Nine Power source

10 Cutoff Circuit

11 Actuation Circuit

A1 AND circuit

F1 Latch circuit

R1 Resistance

Z2 Load

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[Translation done.]

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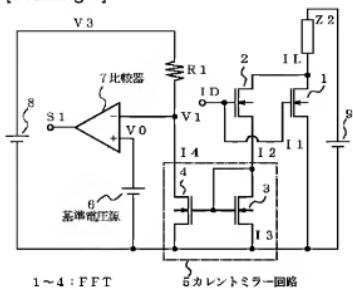
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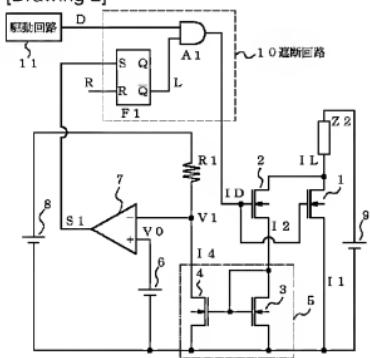
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DRAWINGS

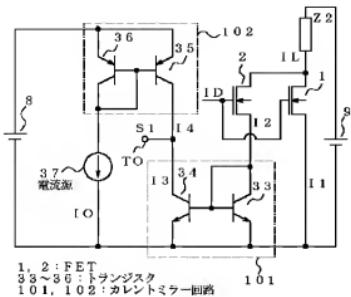
[Drawing 1]



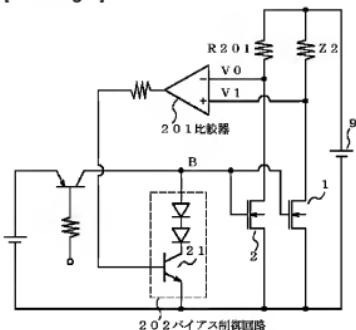
[Drawing 2]



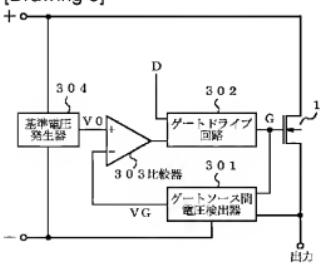
[Drawing 3]



[Drawing 4]



[Drawing 5]



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[Translation done.]

(51) Int.Cl.<sup>6</sup>  
 H 03 K 17/08  
 H 02 H 3/087  
 H 03 K 17/12

識別記号

F I  
 H 03 K 17/08  
 H 02 H 3/087  
 H 03 K 17/12

C

審査請求 有 請求項の数3 O.L. (全6頁)

(21)出願番号 特願平9-126948

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(22)出願日 平成9年(1997)5月16日

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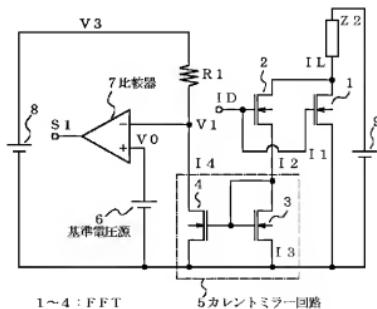
(74)代理人 弁理士 京本 直樹 (外2名)

## (54)【発明の名称】 半導体集積回路装置

## (57)【要約】

【課題】異常検出精度が高くノイズ干渉に強く熱破壊要因を除去しかつインダクタンス成分を含む負荷に対しても負荷状態検出を可能とする。

【解決手段】負荷電流  $I_L$  を制御する出力用のFET  $T_1$  と、負荷電流  $I_L$  の変化分  $I_2$  を抽出するFET  $T_2$  とカレントミラー回路  $5$  と、抽出した電流  $I_2$  対応の電流  $I_4$  を検出電圧  $V_1$  に変換する抵抗  $R_1$  と、検出電圧  $V_1$  と、基準電圧  $V_0$  とを比較し比較信号  $S_1$  を出力する比較器  $7$  とを備える。



## 【特許請求の範囲】

【請求項1】 負荷に接続されこの負荷の負荷電流を制御する出力用の半導体素子と、前記負荷電流の変化分を抽出する負荷電流変化抽出手段と、

抽出した前記負荷電流の変化分を電流変化電圧信号に変換する電流電圧変換手段と、前記電流変化電圧信号と予め定めた基準電圧とを比較し比較信号を出力する電圧比較手段とを備えることを特徴とする半導体集積回路装置。

【請求項2】 前記負荷電流変化抽出手段が、ドレインとゲートの各々を前記半導体素子である第1のFETのドレインとゲートの各々に並列接続しゲート面積が予め定めた比率で前記第1のFETより小さい第2のFETと、

入力端が前記第2のFETのソースに接続したカレントミラー回路とを備え、前記電流電圧変換手段が、一端が前記カレントミラー回路の出力端に他端が電源に接続した抵抗を備えることを特徴とする請求項1記載の半導体集積回路装置。

【請求項3】 前記比較信号の供給に応答して前記半導体素子の駆動信号を遮断する駆動信号遮断手段をさらに備えることを特徴とする請求項1記載の半導体集積回路装置。

## 【発明の詳細な説明】

## 【0001】

【発明の属する技術分野】 本発明は半導体集積回路装置に関し、特に制御系と大電流の出力段素子とを集積化したパワーIC用の半導体集積回路装置に関する。

## 【0002】

【従来の技術】 従来、この種のパワー半導体を用いた半導体集積回路においては、過電流や短絡などによりパワー半導体が破壊するのを防止するための保護機能を有している。

【0003】 この種の保護機能用のモニタ信号生成回路を含む特開平1-193909号公報記載の従来の第1の半導体集積回路装置を回路図で示す図3を参照すると、この従来の第1の半導体集積回路装置は、ドレインが負荷Z2に接続した電圧制御型パワー半導体素子であるFET1と、ドレイン及びゲートがそれぞれFET1のソース及びゲートに並列接続した電流容量の小さい半導体素子であるFET2と、NPN形のトランジスタ33、34から成るカレントミラー回路101と、PNP形のトランジスタ35、36から成るカレントミラー回路102と、トランジスタ36に基準電流I0を供給する電流源37と、カレントミラー回路102に電源を供給する電源8と、FET1、2の電源9とを備える。

【0004】 次に、図3を参照して、従来の第1の半導体集積回路装置の動作について説明すると、FET2のドレイン電流をカレントミラー回路101で受け、基準

電流I0対応のカレントミラー回路102の出力と比較し、差電流対応の電圧信号S1を出力端子TOに出力する。

【0005】 この回路は、パワーFET1と、電流容量の小さいFET2とが並列になるように接続しているため、負荷Z2に流れる電流ILはFET1とFET2の面積比率となるような電流I1、I2に分割され、これら電流I1、I2の各々がFET1とFET2とにそれぞれ分かれ流れることがある。電流I2がFET2へ流れるとき、この電流I2はカレントミラー回路101のトランジスタ33へ流れ込むことにより、トランジスタ34には、トランジスタ33、34の面積比率で決まる電流I3が流れる。また、カレントミラー回路102のトランジスタ36に流れる電流は電流源37によって一定の値となっており、トランジスタ35、36の面積比率で決まる電流I4がトランジスタ35に流れる。したがって、トランジスタ34には負荷R2に流れる電流I1の状態に比例して変化する電流I3が流れるのに対し、トランジスタ34には、ある一定値の電流I4しか流す能力がない。したがって、電流I4に比べて電流I3が小さい場合は、トランジスタ34はトランジスタ35の設定電流I4を流し続けることが出来なくなるために電流の余剰が発生し、この余剰電流をなくすためにトランジスタ35は非飽和領域から飽和領域へと動作点が移るため、出力端子TOの電圧レベルS1は上昇をする。逆に電流I4に比べて電流I3が大きい場合は、トランジスタ34は設定電流I4以上は流すことが出来ないために電流の不足が発生し、この不足分がなくなるようトランジスタ34は非飽和領域から飽和領域へと動作点が移るため、出力端子TOの電圧レベルS1は下降する。

【0006】 以上説明したように、出力端子TOの電圧レベルS1はトランジスタ34、35に流れる電流値I3、I4の大小関係によって変化をする。これにより基準電流I0とカレントミラー回路101、102各々の各トランジスタ33、34及び35、36の面積比率を設定することにより、FET1に流れる電流I1が設定電流値I0になった場合の出力端子TOの電圧レベルS1の変化を利用してFET1の過負荷状態検出を実現する。

【0007】 次に、特開平2-44693号公報記載の従来の第2の半導体集積回路装置を図4と共通の構成要素には共通の文字/数字を用いて同様に回路図で示す図4を参照すると、この従来の第2の半導体集積回路装置は、従来の第1の技術と共通のただしソース及びゲート同志を並列接続したFET1、2と、FET1のドレインと電源9との間の負荷Z2と、電源9とに加えて、FET2のドレインと電源9との間に接続しFET2のドレイン電流対応の基準電圧V0を生成する基準用の抵抗R201と、負荷Z2に生じた負荷電圧V1と基準電

圧V2とを比較し比較信号VSを出力する比較器201と、FET1、2のゲートのバイアス電圧を制御するバイアス制御回路202とを備える。

【0008】次に、図4を参照して、従来の第2の半導体集積回路装置の動作について説明すると、FET1とFET2は、各々の面積比率の逆数K1、K2(K1<K2)にそれぞれ対応したオン抵抗となっている。また、FET1の負荷Z2の抵抗値r2に対し、FET2の負荷抵抗R201の抵抗値r1を $((K2-1) \times R2)$ と設定することにより、通常負荷時は常にFET2のソースドレイン間電圧すなわち基準電圧V0の方がFET1のソースドレイン間電圧すなわち負荷電圧V1よりも高い状態となる。これら電圧V1、V0を比較器201の正及び反転入力に供給し比較信号S1はLレベルを出力する。バイアス制御回路202は比較信号S1のLレベルに応答してトランジスタ21が遮断し、FET1、2のバイアス電圧Bを通常レベルに保持する。この通常負荷状態に対して何らかの原因で負荷Z2の抵抗値が低下した場合、基準電圧V0よりも負荷電圧V1の方が高い状態となる。比較器201は負荷電圧V1の上昇に応答して比較信号S1を反転しHレベルとする。この比較信号S1のHレベルに応答してバイアス制御回路202のトランジスタ22が導通し、バイアス電圧Bを低下させる。このように、電圧V1、V0を比較器201で比較することにより、通常負荷状態と異常負荷状態の検出を実現している。

【0009】次に、特開平3-195212号公報記載の従来の第3の半導体集積回路装置を図3と共に構成要素には共通の文字/数字を用いてブロックで示す図5を参照すると、この従来の第3の半導体集積回路装置は、従来の第1の技術と共にFET1と、FET1のゲートソース間に接続しゲートソース間電圧対応の検出電圧VGを出力する電圧検出器301と、比較信号S2の制御により入力信号Dを増幅してFET1のゲートのドライブ信号Gを供給するゲートドライブ回路302と、基準電圧V0と電圧VGとを比較し比較信号S2を出力する比較器303と、基準電圧V0を発生する基準電圧発生器304とを備える。

【0010】次に、図5を参照して、従来の第3の半導体集積回路装置の動作について説明すると、この回路は、ゲートドライブ回路302の出力Gのレベルを可変させることにより、ゲートソース間電圧とドレイン電流との飽和領域特性を利用することにより所望の電流制限を行うものである。まず、比較器303はゲート検出電圧VGと基準電圧V0とを比較し、ゲートソース間電圧が基準電圧V0よりも大きくならないようドライブ信号Gを制御する。このようにしてゲートドレイン間電圧を設定することにより、FET1のドレイン電流は静特性により決まる電流値以上を流すことができなくなり、FET1のドレイン電流の制限を可能とする。

### 【0011】

【発明が解決しようとする課題】上述した従来の第1の半導体集積回路装置は、2段のカレントミラー回路の各々で生ずる電流誤差が、基準電流値及び過電流検出用の小電流容量の半導体素子に流れる電流値にそれぞれ影響を及ぼし、誤差の原因となるという欠点があった。

【0012】また、上記カレントミラー回路を構成する通常のバイポーラトランジスタでは、活性領域におけるエミッタコレクタ間のインピーダンスは数MΩオーダーであり、したがって出力端子におけるインピーダンスが数MΩとなり、スイッチング時に発生するスイッチングノイズ等が容量結合により出力信号ラインに影響を及ぼして誤動作を発生するという欠点があった。

【0013】また、従来の第2の半導体集積回路装置は、負荷がインダクタンス成分を含む場合、ターンオフ時に発生する逆起電力によりコンバレータの入力端子には電源電圧以上の電圧が印加されるため、ラッチアップ等が発生して素子破壊に至るという欠点があった。

【0014】さらに、従来の第3の半導体集積回路装置は、電圧駆動型半導体素子の飽和特性を利用してはいるが、飽和領域で動作させるためにパワー半導体における電力消費が著しく増加し、過電流による破壊を防止できただとしても、熱破壊に至るという欠点があった。

【0015】本発明の目的は、上記従来技術の持つ問題点を解決し、過負荷等の異常検出精度が高くノイズ干渉に強く熱破壊要因を除去しかつインダクタンス成分を含む負荷であってもパワー半導体素子の状態検出を可能とする半導体回路装置を提供することにある。

### 【0016】

【課題を解決するための手段】本発明の半導体集積回路装置は、負荷に接続されこの負荷の負荷電流を制御する出力用の半導体素子と、前記負荷電流の変化分を抽出する負荷電流変化抽出手段と、抽出した前記負荷電流の変化分を電流変化電圧信号に変換する電流電圧変換手段と、前記電流変化電圧信号と予め定めた基準電圧とを比較し比較信号を出力する電圧比較手段とを備えて構成されている。

### 【0017】

【発明の実施の形態】次に、本発明の第1の実施の形態を図9と共に構成要素には共通の文字/数字を用いて回路図で示す図1を参照すると、この図に示す本実施の形態の半導体集積回路装置は、ドレイン同志及びゲート同志を並接続した従来の第1の技術と共にパワーユニットであるFET1、検出用の小電流素子であるFET2と、電圧V3を供給する電源8と、負荷電流I1を供給する電源9と、負荷用の抵抗R2とに加えて、NチャネルMOS形トランジスタであるFET3、4とから成るカレントミラー回路5と、電源8とFET4のドレインとの間に接続し検出電圧V1を生成する抵抗R1と、基準電圧V0を供給する基準電圧源6と、正入力に

基準電圧  $V_O$  を反転入力に検出電圧  $V_1$  をそれぞれ入力しこれら電圧  $V_O$ ,  $V_1$  の比較を行い比較信号  $S_1$  を出力する比較器 7 とを備える。

【0018】次に、図1を参照して本実施の形態の動作について説明すると、まず、FET1、FET2の各々

$$I1 = IL \times A1 / (A1 + A2) \dots \dots \dots \dots \dots \dots \dots \quad (1)$$

$$J2 \equiv J1 \times A2 / (A1 + A2) \dots \dots \dots \dots \dots \dots \dots \quad (2)$$

電流  $I_2$  は、カレントミラー回路 5 の FET 3 に流れ、FET 4 には FET 3, 4 の各々の素子面積  $A_3, A_4$

$$J4 \equiv J2 \times A4 / (A3 \pm A4) \quad \dots \dots \dots \dots \dots \dots \quad (3)$$

この電流  $I_4$  は FET 4 と電源 8 の間の抵抗  $R_1$  に流れ、この抵抗の抵抗値を  $R_1$  とすると、抵抗  $R_1$  と FET 4 を接続点である箇所 N1 に、次式で表す検出電圧  $V_1$

$$= V3 = [B \times (1 \times A2 \times A4 \setminus \{(A1+A2) \times A3\})] \cup (5)$$

すなわち、検出電圧  $V_1$  は負荷電流  $I_L$  の状態に応じて変化する。

【0022】比較器7は、検出電圧V1と基準電圧VOとを比較し、出力端子TOにこれら電圧VO, V1の大小関係に応応する比較信号S1を出力する。

【0023】ここで、負荷電流  $I_L$  の上限値が負荷  $Z_2$  に流れたとき、検出電圧  $V_1$  と基準電圧  $V_0$  とが等しくなるように各素子の形状及び回路定数を設定する。これにより、設定上限値よりも負荷電流  $I_L$  が小さいすなわち通常状態と、設定上限値を越えて負荷電流  $I_L$  が流れる場合すなわち過負荷状態とで検出電圧  $V_1$  と基準電圧  $V_2$  との大小関係が反転することにより、比較信号  $S_1$  の出力レベルが大きく変化することにより、FET 1 の非駆動を行なう。

【0024】すなわち、通常状態では検出電圧V1は基準電圧V0よりも小さいので比較信号S1はLレベルとなる。過負荷状態では、逆に、検出電圧V1が基準電圧V0よりも大きくなるので比較信号S1はHレベルに反転する。

【0025】具体的な数值例としてFET1, 2の面積比A1:A2を999:1カレントミラー回路5のFET3, 4の面積比A3:A4を10:1, 抵抗R1の抵抗値を2.5kΩ, 基準電圧V0を2.5V, 電源8の電圧V3を5Vとする。また、負荷Z2としては直流等価抵抗の十分に低いインダクタンスを接続しているものとする。

【0026】この状態でFET1, 2に駆動信号IDが供給され、FET1, 2は遮断状態から導通状態になったとき、負荷Z2からは時間経過と共に増加する負荷電流I1が流れ始め、負荷電流I1が9mAまで到達した状態を想定する。この時、FET1, 2には面積比率に応じた電流I1, I2が流れ、(1), (2)式より電流I1は8.991mA、電流I2は9mAとなる。電流I2はそのままカレントミラー回路5に流れため、(3), (4)式よりFET3の電流I3=9mA、FET4の電流I4=8.991mAとなる。

の電流  $I_1, I_2$  は、従来の第1の技術で上述したように、負荷  $Z$  を流れる負荷電流  $I_L$  を FET 1, FET 2 の各々の素子面積  $A_1, A_2$  の比と成るように配分され、それぞれ次式で表される。

[0019]

..... ( 1 )

..... (2)

の比で決定される次式の電流  $I_4$  が

(0020)

### 1 が発生する

100211

1000000000

3133-3134

$$t(A1 + A2)$$

ET4の電流I4は0.9mAとなる。この電流I4は抵抗R1によって検出電圧V1に変換され、この電圧V1は(4)式より2.75Vになり比較器7の反転入力に供給される。これに対し、比較器7の正入力電圧は基準電圧V0の2.5Vであるので、比較器はLレベルを出力する。

【0027】次に、上記の回路状態より時間的に経過して、負荷電流  $I_1$  が  $1.0\text{ A}$  をわずかに越える電流  $1.0\text{ A} + \alpha$  の状態を想定する。この時、電流  $I_1$  は  $9.990\text{ mA} + \alpha\text{ A}$ 、電流  $I_2$  は  $1.0\text{ mA} + \alpha\text{ }2$ 、電流  $I_3$  は  $1.0\text{ mA} + \alpha\text{ }2$ 、電流  $I_4$  は  $1\text{ mA} + \alpha\text{ }3$  となる。この電流  $I_4$  が抵抗  $R_1$  によって検出電圧  $V_1$  に変換され、この検出電圧  $V_1$  すなはち比較器  $7$  の反転入力電圧は  $2.5\text{ V} - \alpha\text{ }4$  になる。これに対し、比較器  $7$  の正入力電圧は基準電圧  $2.5\text{ V}$  のままであり、反転入力の電圧よりも正入力の電圧の方がわずかに高くなるため、比較信号  $S_1$  は反転して H レベルとなる。この比較信号  $S_1$  のレベルを監視することにより、FET  $1$  が過電流状態となっていないか等の状態を検出可能である。

【0028】また、従来の第1の技術ではカレントミラー回路2段で構成しているのに対し、本実施の形態ではカレントミラー回路が1段であるので、カレントミラー回路で生ずる電流誤差の影響が低減できる。また、本実施の形態の回路中で、数MΩオーダーという高いインピーダンスとなっている場所はなく、スイッチングノイズ等による誤動作に対するマージンを拡大することができる。

【0029】さらに、従来の第2の技術のように負荷が抵抗に限定されることはなく、インダクタンス負荷も扱うことが可能である。

【0030】また、本実施の形態において、カレントミラー回路を構成するトランジスタとしてNチャネルMOS形のFETを用いる代わりに、NPNバイポーラ形トランジスタを用いてもよい。

【0031】次に、本発明の第2の実施の形態を図1と共通の構成要素には共通の文字／数字を用いて同様に回

路図で示す図2を参照すると、この図に示す本実施の形態の第1の実施の形態との相違点は、比較信号S1のHレベルへの反転に応答してFET1、2の駆動信号IDを遮断する遮断回路10をさらに付加したことである。【0032】遮断回路10は、比較信号S1をラッチしラッチ信号Lを出力するRSフリップフロップ等のラッチ回路F1と、駆動回路11から供給されるドライブ信号Dとラッチ信号Lとの論理積を取り駆動信号IDを生成する2入力のAND回路A1とを備える。

【0033】動作について説明すると、起動時にラッチ回路F1はリセット信号Rにより初期状態すなわち信号QバーをHレベルにセットする。ラッチ回路F1は入力Sに供給を受けた比較信号S1に応答してこの信号S1をラッチし、反転出力信号QバーをAND回路A1の一方の入力に供給する。AND回路A1はこの信号Qバーと他方の入力に供給を受けたドライブ信号Dとの論理積を取り駆動信号IDを出力する。通常動作状態では、上述のように、比較信号S1はLレベルであるので、信号QバーはHレベルとなりAND回路A1はドライブ信号Dを通過させ駆動信号IDとして出力する。したがって、FET1、2はドライブ信号IDのレベルにしたがって動作する。

【0034】次に、過負荷状態では、比較信号S1はHレベルとなり、信号QバーはLレベルとなるのでAND回路A1はドライブ信号D、したがって駆動信号IDを遮断する。この結果、FET1、2は遮断状態となり、保護動作が実現される。

【0035】FET1、2が遮断したことにより、負荷Z2及びFET3、4に電流を供給することは出来なくなる。しかしこれらFET1、2の遮断とほぼ同時に、比較信号S1はHレベルから再びLレベルへと変化することにより、ラッチ回路F1の入力SはHレベルからLレベルへと変化する。しかし、信号Qバーは、リセット信号Rが入力されるまでLレベルを保持し続けることとなり、ドライブ信号Dとは無関係にFET1、2は遮断状態を保持し続け、FET1、2を保護する。

【0036】本実施の形態の回路は、従来の第3の技術のように、パワーFETの飽和特性を利用するのではなく、パワーFET自体を遮断させるという動作のため、消費電力の急激な増加による発熱によって素子が破壊するということはない。

【0037】

【発明の効果】以上説明したように、本発明の半導体集積回路装置は、負荷電流変化抽出手段と、電流電圧変換手段と、電圧比較手段とを備えているので、カレントミラー回路を1段に削減したためより高精度で半導体素子の状態検出が可能であるという効果がある。

【0038】また、回路中に高インピーダンスとなる部分がないためスイッチングノイズ等の外乱ノイズによる誤動作マージンが大きくできるという効果がある。

【0039】また、負荷の電位変化を直接検出せず、電流変化として抽出してから電圧に変換して検出するため、負荷インピーダンス状態の影響を回避できるので、負荷として抵抗だけではなくインダクタンスも接続可能という効果がある。

【0040】さらに、電圧制御型半導体素子を飽和領域で制御するのではなく、完全に遮断することにより半導体素子内での損失増加による熱破壊を防止できるという効果がある。

【図面の簡単な説明】

【図1】本発明の半導体集積回路装置の第1の実施の形態を示す回路図である。

【図2】本発明の半導体集積回路装置の第2の実施の形態を示す回路図である。

【図3】従来の第1の半導体集積回路装置の一例を示す回路図である。

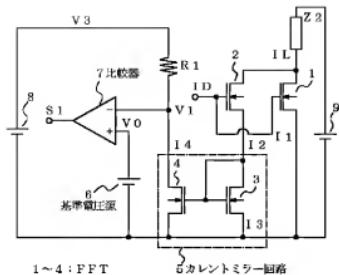
【図4】従来の第2の半導体集積回路装置の一例を示す回路図である。

【図5】従来の第3の半導体集積回路装置の一例を示すブロック図である。

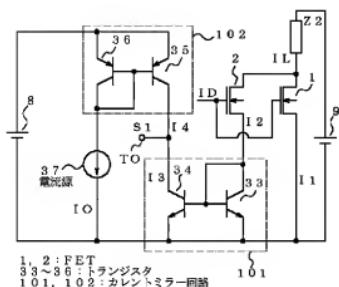
【符号の説明】

1~4	FET
21, 33~36	トランジスタ
5, 101, 102	カレントミラー回路
6	基準電圧源
7, 201, 303	比較器
8, 9	電源
10	遮断回路
11	駆動回路
A1	AND回路
F1	ラッチ回路
R1	抵抗
Z2	負荷

【図1】

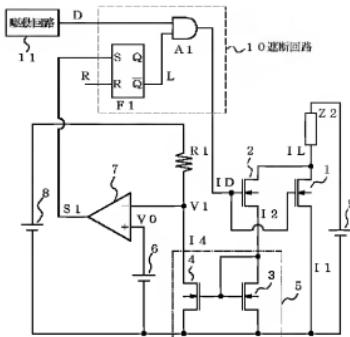


【附3】



【図5】

## 【图2】



【図4】

